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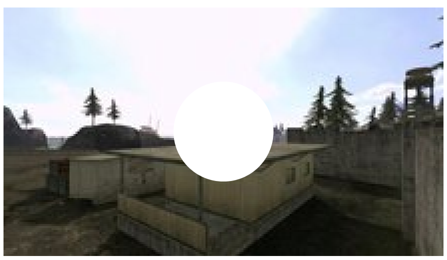
Ray-tracing hardware

Ray-tracing hardware is special-purpose computer hardware designed for accelerating ray tracing calculations.



Quake Wars: Ray Traced was rendered by using now cancelled Intel's Xeon Phi PCI 3.0 board.

Introduction: Ray tracing and rasterization

The problem of rendering 3D graphics can be conceptually presented as finding all intersections between a set of "primitives" (typically triangles or polygons) and a set of "rays" (typically one or more per pixel).[1]

Up to 2010, all typical graphic acceleration boards, called graphics processing units (GPUs), used rasterization algorithms. The ray tracing algorithm solves the rendering problem in a different way. In each step, it finds all intersections of a ray with a set of relevant primitives of the scene.

Both approaches have their own benefits and drawbacks. Rasterization can be performed using devices based on a stream computing model, one triangle at the time, and access to the complete scene is needed only once.[a] The drawback of rasterization is that non-local effects, required for an accurate simulation of a scene, such as reflections and shadows are difficult; and refractions[2] nearly impossible to compute.

The ray tracing algorithm is inherently suitable for scaling by parallelization of individual ray renders.[3] However anything other than ray casting requires recursion of the ray tracing algorithm (and random access to the scene graph) to complete their analysis,[4] since reflected, refracted, and scattered rays require that various parts of the scene be re-accessed in a way not easily predicted. But it can easily compute various kinds of physically correct effects, providing much more realistic impression than rasterization.[b]

The complexity of a well implemented ray tracing algorithm scales logarithmically;[c] this is due to objects (triangles and collections of triangles) being placed into BSP trees or similar structures, and only being analyzed if a ray intersects with the bounding volume of the binary space partition.[5][d]

Implementations

Various implementations of ray tracing hardware have been created, both experimental and commercial:

- (1996) Researchers at Princeton university proposed using DSPs to build a hardware unit for ray tracing acceleration, named "TigerSHARK".[6]
- Implementations of volume rendering using ray tracing algorithms on custom hardware were carried out in 1999 by Hanspeter Pfister[7] and researchers at Mitsubishi Electric Research Laboratories.[8] with the vg500 / VolumePro ASIC based system and in 2002 with FPGAs by researchers at the University of Tübingen with VIZARD II[9]
- (2002) The computer graphics laboratory at Saarland University headed by Dr. -Ing Slusallek has produced prototype ray tracing hardware including the FPGA based fixed function data

driven SaarCOR (Saarbrücken's Coherence Optimized Ray Tracer) chip[10][11][12] and a more advanced programmable (2005) processor, the Ray Processing Unit (RPU)[13]

- (2002–2009) ART VPS company (founded 2002[14]), situated in the UK, sold ray tracing hardware for off-line rendering. The hardware used multiple specialized processors that accelerated ray-triangle intersection tests. Software provided integration with Autodesk Maya and Max data formats, and utilized the Renderman scene description language for sending data to the processors (the .RIB or Renderman Interface Bytestream file format).[15] As of 2010, ARTVPS no longer produces ray tracing hardware but continues to produce rendering software.[14]
- (2009 - 2010) Intel[16] showcased their prototype "Larrabee" GPU and Knights Ferry MIC at the Intel Developer Forum in 2009 with a demonstration of real-time ray-tracing.
- Siliconarts[17] developed a dedicated real-time ray tracing hardware (2010). RayCore (2011), which is the world's first real-time ray tracing semiconductor IP, was announced.
- Caustic Graphics[18] have produced a plug in card, the "CausticOne" (2010), that accelerates global illumination and other ray based rendering processes when coupled to a PC CPU and GPU. The hardware is designed to organize scattered rays (typically produced by global illumination problems) into more coherent sets (lower spatial or angular spread) for further processing by an external processor.[19]
- Imagination Technologies, after acquiring Caustic Graphics, produced the Caustic Professional's R2500 and R2100 plug in cards containing RT2 ray trace units (RTUs). Each RTU was capable of calculating up to 50 million incoherent rays per second.[20]
- Nvidia, partnering with Microsoft DirectX, announced the Nvidia RTX developer library[21] in 2018, which promised fast real-time ray tracing solutions powered by hardware accelerated ray tracing (ASIC tensor cores) found in the Volta-generation GPUs.[22]
- In October 2020, AMD announced further information regarding the "refresh" of the RDNA micro-architecture. According to the company, the RDNA 2 micro-architecture supports real-time hardware accelerated ray tracing.[23][24]

Notes

a. *For additional visualisations such as shadows, or reflections such as produced by a large flat body of water an addition pass of the scene graph is required for each effect.*

b. *Rasterisation methods are capable of generating realistic shadows (including shadows produced by partially transparent objects), and plane reflections easily (as of 2010), but do not easily implement* *reflections from non planar surfaces (excluding approximations using normal maps) or refractions.*

c. *That is if X is the number of triangles, then the number of computations to complete the scene is proportional to log(X).*

d. *The same methods can be used in rasterization; in a simplistic implementation, culling is limited to those BSP partitions that lie within the much larger viewing frustum (more advanced implementations including those that implement occlusion culling or predicated rendering scale better than linearly for complex (especially high occluded) scenes (Note in common API's : DirectX 10 D3D10_QUERY_OCCLUSION_PREDICATE [1] (http://msdn.microsoft.com/en-us/library/ee415853(VS.85).aspx) , in OpenGL 3.0 HP_occlusion_query). With ray tracing the viewing frustum is replaced by the volume enclosed by a single ray (or ray bundle).*

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Further reading

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